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EDUCATION

New York University, MS in Computer Engineering | CGPA: 3.87/4.0 **Sept 2024 – May 2026**
Coursework: Generative AI Based Chip Design, System-on-Chip Design, Computing Systems Architecture, VLSI Systems & Architecture, Analog IC Design

College of Engineering Guindy, Anna University, BE Electronics and Communication Engineering | CGPA: 8.51/10 **Sept 2020 – May 2024**

Coursework: Digital System Design, Digital VLSI, Linear ICs, Operating Systems, Machine Learning, Advanced Microcontrollers

SKILLS

Languages: SystemVerilog, Verilog, Python, Tcl

Verification: UVM, Constrained-Random Verification, SystemVerilog Assertions (SVA), Assertion-Based Verification, Functional & Code Coverage, Coverage Closure, Scoreboarding, Reference Modeling

Tools: Cadence Xcelium, SimVision, IMC, Synopsys VCS, Design Compiler, Genus, Innovus, Virtuoso, OpenLane, Xilinx Vivado, Linux, Git, Make

Hardware Concepts: RTL Design, Microarchitecture, Clock Domain Crossing (CDC), Static Timing Analysis (STA)

PROJECTS

Verification of a Burst-Capable AXI4 Slave Using SystemVerilog and UVM

- Built a **UVM environment** (driver, monitor, reference-model scoreboard, functional coverage) verifying AXI4 FIXED/INCR/WRAP bursts, byte-lane strobes, and error responses across 8 tests on **Cadence Xcelium**.
- Wrote **14 SystemVerilog Assertions** for channel handshake, payload stability, and reset protocol compliance; achieved **100% functional coverage** via constrained-random and directed error-injection stimulus.
- Found and root-caused **3 RTL bugs** - a response-flag race condition, a write-FSM deadlock on early WLAST, and an error-path memory-corruption bug - using a strict **per-beat scoreboard** and **directed error injection**.

Assertion-Based Verification of a Dual-Clock Asynchronous FIFO for CDC

- Designed and verified a **parameterized dual-clock asynchronous FIFO** (Gray-code pointers, 2-flop CDC synchronizers, MSB-invert full/empty logic) with a **self-checking SystemVerilog testbench** and a **14-assertion / 8-cover-property SVA suite** (bind-attached, race-free clocking-block sampling, reference-queue scoreboard) regressed across **5 clock-ratio scenarios** on **Cadence Xcelium**.
- Root-caused a same-edge **race condition** between the write- and read-clock-domain stimulus shutdown paths that could silently drop an in-flight write during drain; fixed it by decoupling the **write/read enables** for a guaranteed **lossless drain**.

LLM-Assisted Verification Assistant Using LangChain, LangGraph, and RAG

- Built a **RAG pipeline** over the 500-page ARM AXI4 specification using **LangChain**, **ChromaDB**, and Claude with regex preprocessing, semantic chunking, and **MMR retrieval** for grounded spec Q&A.
- Designed agentic coverage gap analyzer in **LangGraph** that parses functional coverage reports and suggests **UVM constrained-random stimulus** to close uncovered bins.

Functional Verification of SPI Protocol Using SystemVerilog and UVM

- Developed **UVM environment** for an SPI controller with constrained-random read/write transactions and **functional coverage** tracking CPOL, CPHA modes.
- Designed **self-checking scoreboard** using a 32×8 reference memory model validating readback correctness through reset recovery and corner-case timing scenarios.

EXPERIENCE

New York University | New York, USA

June 2025 - May 2026

Course Assistant | VLSI System & Architecture Design

- Automated a Python grading pipeline that batch-compiles and simulates student RTL submissions in **Synopsys VCS** and generates structured pass/fail reports.
- Prepared hands-on lab manuals and assignments for schematic/layout and digital design; debugged student RTL and testbench issues during lab hours.